1. (a) Discuss about Flynn’s classification of computers.
   (b) Explain about communication topologies used in multiprocessors. [16]

2. Write about direct, indirect, register direct, register indirect, immediate, implicit, relative, index, and base address mode of addressing. Why do we need so many addressing modes? Is the instruction size influenced by the number of addressing modes which a processor supports? State whether the number of addressing modes will be more in RISC or CISC? [16]

3. (a) Why do we need subroutine register in a control unit? Explain. [8]
   (b) Explain nanoinstructions and nanometry. Why do we them? [8]

4. Explain the computational errors. Why do they occur?. Give some problems where these errors are catastrophic. Also, give some practical examples (algorithms) where error gets
   (a) accumulated and
   (b) multiplies. [16]

5. Explain the following with applications for each:
   (a) ROM
   (b) PROM
   (c) EPROM
   (d) EEPROM. [4+4+4+4]

6. Explain the following:
   (a) Isolated Vs Memory mapped I/O
   (b) I/O Bus Vs Memory Bus
   (c) I/O Interface
   (d) Peripheral Devices. [4+4+4+4]

7. (a) What is pipelining? Explain. [8]
   (b) Explain four segment pipelining. [8]
8. (a) Explain multiport memory organization with a neat sketch.
(b) Explain system bus structure for multiprocessors with a neat sketch. [8+8]
III B.Tech I Semester Regular Examinations, November 2007
COMPUTER ORGANISATION
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Electronics & Control Engineering and Electronics & Telematics)
Time: 3 hours Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) Explain about various buses such as internal, external, backplane, I/O, system, address, data, synchronous and asynchronous.
   (b) Distinguish between high level and low level languages? What are the requirements for a good programming language?

2. Design register selection circuit to select one of the four 4-bit registers content on to bus. Give fuller explanation.

3. (a) How do we reduce number of microinstructions. What are micro-subroutines?
   (b) Explain nanoinstructions and nanometry. Why do we need them?

4. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove.
   (b) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems.

5. (a) What is the functioning of a Flash Memory? Explain.
   (b) Give the detailed picture of Memory Hierarchy.

6. Explain the following:
   (a) Asynchronous Serial Transfer
   (b) Asynchronous Communication Interface.

7. Explain three segment instruction pipeline. Show the timing diagram and show the timing diagram with data conflict.

8. (a) Explain the working of 8 x 8 Omega Switching network.
   (b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch.
1. Distinguish between error detection and correction codes. What do you understand by odd parity and even parity? What is odd function and even function? To calculate odd and even parity values which functions can be used? Calculate Odd and even parity values for all hexadecimal digits 0-9 and A-F.

2. (a) Explain about stack organization used in processors. What do you understand by register stack and memory stack?
(b) Explain how \( X = (A + B) / (A - B) \) is evaluated in a stack based computer.

3. (a) How do you map micro-operation to a micro instruction address.
(b) Hardwired control unit is faster than microprogrammed control unit. Justify this statement.

4. (a) What is the use of fast multiplication circuits? Write about array multipliers.
(b) Multiply 10111 with 10011 using booth’s algorithm.

5. (a) Explain how the Bit Cells are organized in a Memory Chip.
(b) Explain the organization of a 1K x 1 Memory with a neat sketch.

6. (a) What is Direct Memory Access? Explain the working of DMA.
(b) What are the different kinds of DMA transfers? Explain.
(c) What are the advantages of using DMA transfers?

7. (a) What is pipeline? Explain.
(b) Explain arithmetic pipeline.

8. (a) Explain the working of 8 x 8 Omega Switching network.
(b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch.
1. (a) Explain about various buses such as internal, external, backplane, I/O, system, address, data, synchronous and asynchronous.

(b) Explain about daisy chain based bus arbitration. [16]

2. (a) Design a circuit transferring data from a 4bit register which uses D flip-flops to another register which employs RS flip-flops. [8]

(b) What are register transfer logic languages? Explain few RTL statement for branching with their actual functioning. [8]

3. (a) Support the statement Instruction Set Architecture has impact on the processors microarchitecture. [8]

(b) How do we reduce number of microinstructions? What are micro-subroutines? [8]

4. (a) Draw a flow chart which explains multiplication of two signed magnitude fixed point numbers. [8]

(b) Multiply 10111 with 10011 with the above procedure given (a). Show all the registers content for each step. [8]

5. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain. [16]

6. (a) What is polling? Explain in detail.

(b) What is daisy chaining? Explain. [8+8]

7. (a) What is pipeline? Explain space-time diagram for Pipeline.

(b) Explain pipeline for floating point addition and subtraction. [8+8]

8. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those. [6]

(b) Explain time-shared common bus Organization. [5]

(c) Explain system bus structure for multiprocessors. [5]

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B. Tech III Year II Semester Examinations, April/May - 2012
COMPUTER ORGANIZATION
(Common to EIE, ICE)

Time: 3 hours                     Max. Marks: 75

Answer any five questions
All questions carry equal marks

1.a) Describe i) assembler ii) compiler iii) interpreter
b) Represent decimal number 4593 in
i) Excess – 3 code and ii) as a binary number [15]

b) Write short notes on stock organization. [15]

3.a) What are the functional parts of a micro – instruction format?
b) Draw the block diagram depicting address selection for control memory. [15]

4.a) What are the different methods available for dividing numbers? Explain.
b) Prove that the multiplication of two n-digit numbers in base v gives a product no more than 2n digits in length. [15]

5.a) Show by the means of a block diagram a 8Mx32 memory using 512k x 8 memory chips.
b) Explain i) associative mapping ii) set – associate mapping iii) direct mapping. [15]

6.a) What are the different functions of an I/o interface?
b) What is the basic advantage of using interrupt initiated data transfer over transfer under program control without an interrupt. [15]

7.a) What is a structural hazard? Explain with an example.
b) Give an example of a program that will cause data conflict in a three segment pipeline. [15]

8.a) Explain i) mutual exclusion ii) critical section iii) hardware lock
b) Differentiate between serial arbitration logic and parallel arbitration logic. [15]

*********
1. a) Compare the merits and demerits of assembly language and high level language.
   b) Convert the hexadecimal F3A7C2 to binary and octal.  

2. a) What are the basic differences between a branch instruction, a call subroutine instruction and a program interrupt?
   b) Explain about the program status word. 

3. a) What are the address sequencing capabilities required in a control memory?
   b) Explain with a block diagram the decoding of micro operation fields. 

4. a) Write short notes on Decimal Arithmetic unit.
   b) Draw the flow chart for multiplication of floating point numbers. 

5. a) Write short notes on i) write buffer ii) prefetching .
   b) What are the different types of magnetic memory? Describe each briefly. 

6. a) Explain with a timing diagram an input data transfer using hand shake scheme.
   b) Explain the working of a daisy chain priority interrupt. 

7. a) Explain the basic concepts of instruction pipeline.
   b) What is an array processor? What are the different types of array processors? 

8. a) What is cache coherence and why is it important in shared – memory multiprocessor systems.
   b) Explain i) Cross bar networks ii) Multistage networks 

**********
1.a) What are EBCDIC codes? How many characters can be represented by these codes?
b) Discuss over flow and underflow phenomena which occurs in a digital computer. [15]

2.a) What are the main types of interrupt that cause a break in the normal execution of a program?
b) List the important differences between RISC and CISC architecture. [15]

3.a) Explain the usage of a control address register.
b) What are the various parameters which control a conditional branch decision? [15]

4.a) Show the hardware implementation for Booth’s algorithm.
b) Show that there can be no mantisa overflow after a multiplication operation. [15]

5.a) Discuss the advantages and disadvantages of making the size of the cache blocks larger or smaller.
b) What is memory interleaving? How does it reduce the block transfer time? Explain. [15]

6.a) What is a bus arbitration? Explain
i) centralized arbitration
ii) distributed arbitration.
b) Explain IEEE 1394 standard for high-speed serial data transfer. [15]

7.a) Write short notes on
i) Precise exception
ii) Imprecise exception. What kind of exception is provided in case of external interrupts?
b) Explain Attached array processor. [15]

8.a) Discuss the difference between tightly coupled multiprocessors and loosely coupled multiprocessor from the view point of hardware organization and programming techniques.
b) How does a hypercube interconnection work? [15]

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B. Tech III Year II Semester Examinations, April/May - 2012
COMPUTER ORGANIZATION
(Common to EIE, ICE)

Time: 3 hours                     Max. Marks: 75

Answer any five questions
All questions carry equal marks

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1. a) What is a multi processor system? What are the similarities between a multi processor and a multi computer?
    b) How is a negative number represented? Represent – 7 in a binary format. [15]

2. a) What is the difference between a software interrupt and a sub routine call.
    b) How is the state of the CPU determined at the end of the execute cycle? [15]

3. a) What are the micro instructions needed for a fetch routine?
    b) What are steps that a control must undergo during the execution of a single instruction? [15]

4. a) Implement a 2- circuit by 2 – bit array multiplier using combinational circuit.
    b) Explain with a block diagram for a BCD adder. [15]

5. a) What are replacement algorithms ? Explain any one in detail?
    b) What is a memory is it used? What are its functions? [15]

6. a) Write briefly about i) subroutine ii) interrupt – service routine.
    b) Why does the DMA have priority over the CPU when both request a memory transfer? [15]

7. a) What are the different ways in which branch instructions can be handled to reduce their negative impact on the rate of execution of instructions?
    b) Give an example of a program that will cause a branch penalty in a three - segment pipeline. [15]

8. a) What is the purpose of a system bus controller ? Explain how the systems can be designed to distinguish between references to local memory and references to common shared memory.
    b) What is cache coherence? Explain. [15]

*****
1. (a) Explain about IAS memory formats.
    (b) List various registers in a computer along with their purpose [8+8]

2. (a) Find the output binary number after performing the following arithmetic operations
    i. 111.01 + 10.111
    ii. 11.01 + 110.11
    iii. 110.11 - 111.01
    (b) Explain about the longhand division of binary integers. [6+10]

3. (a) Describe various Pentium data types
    (b) Describe various common data transfer instruction set operations. [6+10]

4. (a) List various R3000 pipeline stages. Also explain the function of each.
    (b) List and describe all shift and multiply/divide instructions of MIPS R-Series processors. [8+8]

5. (a) Differentiate between single versus two-level caches.
    (b) Elaborate on Pentium Cache Organization. [8+8]

6. Discuss three possible techniques for I/O operations with merits and demerits of each. [16]

7. (a) Discuss about I/O channel architecture.
    (b) Discuss about I/O addressing in 8086.
    (c) Discuss the salient features of laser printer [6+6+4]

8. (a) Give a summary of arithmetic and logical operations that are defined for the vector architecture.
    (b) What is cache coherence problem. Discuss about different cache coherence approaches. [8+8]
1. (a) Explain the purpose and merits of interrupts.
   (b) Draw and explain the instruction cycle with interrupts.
   (c) What is interrupt handler? Explain its purpose. [6+6+4]

2. (a) How subtraction is done on the binary numbers represented in one’s complement notation give an examples.
   (b) What do you mean by r’s complement. [8+8]

3. NOOP instruction has no effect on the CPU state other than incrementing the program counter. Suggest some uses of this instruction with examples. [16]

4. Elaborate on different types of registers in a register organization [16]

5. Discuss about address translation with segmentation and paging in the Intel Pentium [16]

6. (a) How would CPU handles multiple devices. Explain with different techniques available
   (b) Discuss the characteristics of Intel 8259A interrupt controller. [8+8]

7. (a) Discuss about I/O channel architecture.
   (b) Discuss about I/O addressing in 8086.
   (c) Discuss the salient features of laser printer [6+6+4]

8. (a) Classify and explain different multiprocessors
   (b) Explain the organization of tightly coupled multiprocessor system with a generic block diagram. [8+8]

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1. (a) Define PCI. Explain the applications of PCI
    (b) Describe any ten mandatory PCI signals. [8+8]

2. Write an algorithm to subtract binary numbers represented in normalized floating point mode with base 2 for exponent [16]

3. NOOP instruction has no effect on the CPU state other than incrementing the program counter. Suggest some uses of this instruction with examples. [16]

4. Elaborate on different types of registers in a register organization [16]

5. Give a block diagram for a 4M×8 memory using 256K×1 memory chips. [16]

6. (a) Explain about magnetic disk layout
    (b) Elaborate on Winchester disk track format. [8+8]

7. (a) Explain about microinstruction format of TI 8800
    (b) Explain about ALU control fields of IBM 3033 microinstruction. [8+8]

8. (a) Explain the following terms.
    i. Read miss
    ii. Read hit
    iii. Write miss
    iv. Write hit
    (b) Discuss different approaches to vector computation [8+8]
1. (a) Discuss the interconnection structure design of a computer.
(b) Explain various bus lines.
(c) What do you mean by multiple-bus hierarchies. [8+4+4]

2. (a) Find the output binary number after performing the arithmetic operation using 1’s complement representation.
   i. 111.01 + 10.111
   ii. 110.11 - 111.01
(b) Explain steps involved in the addition of numbers using 2’s complement notation. [10+6]

3. Discuss about various Pentium addressing modes with algorithms [16]

4. (a) List various R3000 pipeline stages. Also explain the function of each.
(b) List and describe all shift and multiply/divide instructions of MIPS R-Series processors. [8+8]

5. (a) Discuss about address translation in paging.
(b) How does page size effect storage utilization and effective memory data-transfer rate [8+8]

6. Discuss about data organization and formatting of magnetic disk in detail [16]

7. Discuss about horizontal and vertical instruction formats. Also differentiate between horizontal and vertical instruction formats. [16]

8. (a) Explain different types of parallel processors.
(b) What do you mean by compound instruction? Give examples
(c) Elaborate on registers of the IBM3090 vector facility. [4+6+6]
1. (a) Explain about various buses such as internal, external, backplane, I/O, system, address, data, synchronous and asynchronous.

(b) Explain about daisy chain based bus arbitration. [16]

2. (a) Design a circuit transferring data from a 4bit register which uses D flip-flops to another register which employs RS flip-flops. [8]

(b) What are register transfer logic languages. Explain few RTL statement for branching with their actual functioning. [8]

3. (a) Explain the functioning of a control unit explaining the terms control word, control memory, control address register and control buffer register. [8]

(b) Support or oppose the statement ?If we want to add a new machine language instruction to a processors instruction set, simply write a C program and compile and store the resultant code in control memory?. [8]

4. Explain the basis for booths multiplication algorithm along with its constituents steps. What type of numbers it will work?. What are the limitations of the same. What are the HW requirements to realize the same in HW. Give an example for the working of Booth?s algorithm. [16]

5. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain. [16]

6. (a) What is daisy chaining? Explain with neat sketch.

(b) What is parallel priority interrupt method? Explain with neat sketch. [8+8]

7. (a) What is meant by instruction pipeline? Explain four segment Instruction Pipeline.

(b) Give the timing diagram of instruction pipeline. [8+8]

8. What is cache coherence and why is it important in shared memory multiprocessor systems? How can the problem be solved with a snoopy cache controller? [16]
III B.Tech I Semester Regular Examinations, November 2008
COMPUTER ORGANISATION
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Electronics & Control Engineering and Electronics & Telematics)

Time: 3 hours
Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. Distinguish between error detection and correction codes. What do you understand by odd parity and even parity?. What is odd function and even function? To calculate odd and even parity values which functions can be used? Calculate Odd and even parity values for all hexadecimal digits 0-9 and A-F. [16]

2. (a) Identify different types of instructions and describe their formats with their constituent fields. Mention which factors influence the size of the fields. [8]
(b) How do we classify CPU’s based on their register organizations. In which organizations, zero address instructions are used. Mention few zero address instructions and their actual execution in practice. [8]

3. (a) Give the typical horizontal and vertical microinstruction formats. [8]
(b) Describe how microinstructions are arranged in control memory and how they are interpreted. [8]

4. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove. [8]
(b) What is overflow and underflow. What is the reason?. If the computer is considered as infinite system do we still have these problems?. [8]

5. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain. [16]

6. Explain the following:
   (a) Asynchronous Serial Transfer
   (b) Asynchronous Communication Interface [8+8]

7. What is pipelining? Explain pipeline processing with an example. [16]

8. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those. [6]
(b) Explain time-shared common bus Organization [5]
(c) Explain system bus structure for multiprocessors [5]

*****
1. (a) Explain about sign magnitude and 2’s complement approaches for representing
the fixed point numbers. Why 2’s complement is preferable.
(b) Give means to identify whether or not an overflow has occurred in 2s comple-
ment addition or subtraction operations. Take one example for each possible
situation and explain. Assume 4 bit registers.
(c) Distinguish between tightly coupled microprocessors and tightly coupled Mi-
croprocessors.
2. (a) Design a circuit transferring data from a 4bit register which uses D flip-flops
to another register which employs RS flip-flops.
(b) What are register transfer logic languages. Explain few RTL statement for
branching with their actual functioning.
3. (a) What are the major design considerations in microinstruction sequencing?
(b) Explain about microinstruction sequencing techniques, specifically variable
format address microinstruction.
4. (a) Multiply 10111 with 10011 using, Booths algorithm.
(b) Explain booths algorithm with its theoretical basis.
5. (a) A two-way set associative cache memory uses blocks of 4 words. The cache can
accommodate a total of 2048 words from main memory. The main memory
size is 124K x 32
   i. Formulate the information required to construct cache Memory
   ii. What is the size of cache Memory.
(b) The access time of cache memory is 100ns and that of main memory is 1000ns.
   It is estimated that 80% of memory requests are for read and the remaining
   20% for write. The hit ratio for read access only is 0.9. A write through
   procedure is used.
      i. What is the average access time of the system considering only read cycles?
      ii. What is the average access time of the system considering both read and
        write cycles?
6. (a) Explain bit oriented and character oriented protocols in serial communication
(b) What are the different issues behind serial communication? Explain. [8+8]

7. (a) Explain RISC pipeline in detail.
    (b) Explain vector processing [8+8]

8. What are the different kinds of Multi stage Switching networks? Explain with neat sketch. Compare their functioning. [16]

*****
1. (a) Explain about various buses such as internal, external, backplane, I/O, system, address, data, synchronous and asynchronous.
   (b) Explain about daisy chain based bus arbitration. [16]

2. Design register selection circuit to select one of the four 4-bit registers content on to bus. Give fuller explanation. [16]

3. (a) Explain the variety of techniques available for sequencing of microinstructions based on the format of the address information in the microinstruction. [8]
   (b) Hardwired control unit is faster than microprogrammed control unit. Justify this statement. [8]

4. (a) Explain single precision and double precision calculations. In general how many bytes are uses for both and what is the precision we get. Give some examples where double precision calculations are needed. [8]
   (b) Explain booths algorithm with its theoretical basis. [8]

5. Explain two-way set associative mapping and four-way set associative mapping techniques with an example for each. [16]

6. Explain the following:
   (a) Isolated Vs Memory mapped I/O
   (b) I/O Bus Vs Memory Bus
   (c) I/O Interface
   (d) Peripheral Devices [4+4+4+4]

   (b) Explain each stream of the Flynn’s classification with an example. [10]

8. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those. [6]
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Code No: 07A60501
JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B. Tech III Year II Semester Examinations, May – 2013
Operating Systems
(Computer Science and Engineering)

Time: 3 hours  Max. Marks: 80
Answer any five questions
All questions carry equal marks

1. a) What are the high level services provided by an OS? Explain.
  b) Explain about the structure of operating system. [16]

2. Define Starvation. The Scheduling algorithms given below suffer from starvation or not. If yes under what circumstances. Explain with examples.
   a) FCFS  
   b) SJF  
   c) Priority  
   d) Round Robin. [16]

3. Compare semaphore and monitor. Which is the best tool for synchronization? Explain with examples. [16]

4. a) Explain demand paged memory management techniques.
    b) What are the steps in handling a page fault? [16]

5. a) Discuss about the deadlock prevention approach.
    b) Explain about kernel I/O subsystem. [16]

6. a) Explain different types of file access methods.
    b) Explain the following methods of allocating disk space:
       i) Linked allocation  
       ii) Indexed allocation. [16]

7. Suppose the head of a moving head disk with 200 tracks numbered 0 to 199 is currently serving a request at track 145 and has just finished a request at 165. If the queue of requests is kept in the FIFO order 186, 17, 91, 177, 94, 10, 102, 175, 13, 123. What is the total head movement to satisfy these requests for the following disk scheduling algorithms?
   a) FCFS  
   b) SSTF  
   c) SCAN  
   d) LOOK  
   e) C-SCAN. [16]

8. Write short notes on:
   a) Access matrix  
   b) Language based protection  
   c) firewall. [16]

*******
1. a) Describe the characteristic features of the following operating systems.
   a) Time sharing operating system  
   b) Real Time operating system  
   c) Distributed operating system.  

2. a) What are the various criteria for comparing different CPU scheduling algorithms?
    Explain any two algorithms with examples.
   b) What is thread? What are the benefits of multithreaded programming?  

3. Briefly discuss about producer-consumer problem and give a solution using binary semaphore.  

4. a) What is page fault? Explain page fault service routine with a neat diagram.
    b) Explain Belady’s Anomaly.  

5. a) How does the operating system perform the function of Input and Output?
    b) How does the System Recover from Deadlock? Discuss.  

6. a) What are the difficulties involved in allowing users to share files? Discuss.
    b) Explain the different methods of maintaining free space list.  

7. What are the different disk scheduling algorithms? Explain.  

8. a) What are the goals of protection? Explain.
    b) Explain about program Threats.  

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B. Tech III Year II Semester Examinations, May – 2013
Operating Systems
(Computer Science and Engineering)

Time: 3 hours

Answer any five questions
All questions carry equal marks

Max. Marks: 75

1. a) Write briefly on layers in OSI model and IP suite.
   b) Write in detail on an overview of TCP/IP protocols. [8+7]

2. Explain the TCP based client server programming using daytime server/client example. [15]

3. a) Explain the sequence of system call execution in a TCP client-server programming.
   b) Write short notes on protocol usage by common internet applications. [8+7]

4. With suitable diagrams, explain the different I/O models. [15]

5. Write a C program to implement a basic calculator server and a client on port number 2345 using UDP based system-calls. Client request the server in the format of 12+34 and the server responds with the result as 46. Server supports the +, -, *, and / operations. [15]

6. a) Briefly explain the functions getsockopt, setsockopt, fcntl and ioctl.
   b) Write a program that displays all IP addresses of a given domain name. [7+8]

7. Write in detail on the signatures and applications of semaphores and message queues. [15]

8. Explain the functions gethostbyname, gethostbyaddr, getservbyname and getservbyport giving the signatures and applications. [15]
1.a) What is an operating system? Discuss the various functions of operating system.
b) What are the benefits of Multithreaded Programming? [8+7]

2.a) What is the use of process table in process management? How does OS update a process table?
b) Explain how does priority scheduling differ from round robin method? [8+7]

3.a) What is a semaphore? Explain the Critical Section (CS) implementation with Semaphores?
b) Define critical-section problem? Give a classical peterson’s solution to the critical section problem? [8+7]

4. Explain the concept of Least Recently Used memory page replacement method and how it is different from First In First Out (FIFO) page replacement method? [15]

5.a) Why is deadlock detection much more expensive in a distributed environment than in a centralized environment?
b) Explain Banker’s algorithm to handle deadlocks? [8+7]

6.a) Discuss the file protection mechanisms incorporated in a Unix file system
b) Why do some systems keep track of the type of a file, while others leave it to the user or simply do not implement multiple file types? Which system is “better”? [7+8]

7.a) What are the advantages of Contiguous allocation? What are the drawbacks of contiguous allocation of disk space?
b) Write the principles that may be employed to improve the efficiency of I/O operations? [8+7]

8.a) Why is it difficult to protect a system in which users are allowed to do their own I/O? Explain how relocation helps for the protection of the data?
b) Explain how cryptography is used as a security tool? [7+8]
III B.Tech I Semester Regular Examinations, November 2007
OPERATING SYSTEMS

Time: 3 hours
Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. Draw and explain program flow of control without and with interrupts. [16]

2. Explain the following transitions:
   (a) Blocked → Blocked/Suspended.
   (b) Blocked/Suspended → Ready/Suspended.
   (c) Ready/Suspended → Ready. [5+5+6]

3. (a) What is a semaphore? What are the various operations defined on it?
    (b) What is the difference between weak semaphore and strong semaphore? Explain. [8+8]

4. (a) Explain the uses of the following:
      i. Event Object
      ii. Mutex Object
      iii. Semaphore Object
      iv. Waitable timer Object.
    (b) Describe about mechanism used by Windows to implement Synchronization of Critical Section objects. [8+8]

5. Explain paging scheme for memory management, discuss the paging hardware and paging model. [16]

6. (a) Explain about the key scheduling criteria.
    (b) Give a detail note on short-term scheduling. [8+8]

7. (a) Explain hash file organization.
    (b) Discuss the address information elements of a file directory. [8+8]

8. Write a note on:
   (a) Access control list of Windows 2000.
   (b) Standard access types of Windows 2000.
   (c) Access tokens of Windows 2000.
1. (a) How can logical address space be contiguous if the physical address space is not contiguous? Explain.
   (b) What is the purpose of TLB?
   (c) What is a paging demon? What does it do?
   (d) Compare swapping and overlays. [4+4+4+4]

2. Write the short notes on the following
   (a) Race Condition
   (b) Process Interaction [8+8]

3. Explain about protection technique of critical section in LINUX. [16]

4. (a) Why is the average search time to find a record in a file less for an indexed sequential file than for a sequential file? Explain.
   (b) What is the difference between a file and a database?
   (c) What are typical operations that may be performed on a directory? [6+4+6]

5. Define Real-time operating systems. Explain their importance in various applications. [16]

6. Draw and explain process state transition diagram with two suspended states. [16]

7. (a) Give the classification of intruders. Explain each class.
   (b) Compare User-Oriented access control with data-oriented access control. [8+8]

8. (a) What is the difference between logical I/O and device I/O?
   (b) Explain feed back scheduling policy. [8+8]

****
Code No: 35068

(a) Give Gantt chart illustrating the execution of these jobs using First-Come-First-Serve, Round-Robin (quantum=1). Shortest process next. Shortest remaining time.

(b) What is the turn around time, waiting time of each jobs for each of the above scheduling algorithms.

7. Explain various file organization and access techniques.

8. (a) Discuss the four stages of a typical virus during its life time.

(b) Differentiate between reactive password checking and proactive password checking techniques.

*****
1. What are the major activities of an operating system with regard to secondary storage management? [16]

2. Draw and explain the Thread structure for Adobe PageMaker. [16]

3. What is a monitor? Explain how it is used in solving critical section problem. [8+8]

4. Explain Reader-Writer Semaphores. [16]

5. (a) A computer has four page frames. The time of loading, time of last access and the R and M bits for each page are as shown below (the times are in clock ticks):

<table>
<thead>
<tr>
<th>Page</th>
<th>Loaded</th>
<th>Last ref</th>
<th>R</th>
<th>M</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>126</td>
<td>279</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>230</td>
<td>260</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>120</td>
<td>272</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>160</td>
<td>280</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

i. Which page will FIFO replace
ii. Which page will LRU replace
iii. Which page will second chance replace

(b) In a fixed-partitioning scheme, what are the advantages of using unequal-size partitions? [9+7]

6. Assume following are the jobs to execute with one processor:

<table>
<thead>
<tr>
<th>Job</th>
<th>Burst Time</th>
<th>Priority</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>8</td>
<td>2</td>
</tr>
<tr>
<td>P2</td>
<td>6</td>
<td>3</td>
</tr>
<tr>
<td>P3</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>P4</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>P5</td>
<td>10</td>
<td>3</td>
</tr>
</tbody>
</table>

The jobs are assumed to have arrived in the order 1, 2, 3, 4, 5
(b) What is cipher feedback mode? Why it is used?

*****